

UTILITY PATENT APPLICATION TRANSMITTAL

(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
YOR9-2000-0175

Total Pages in this Submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

METHOD AND SYSTEM FOR HIGH RESOLUTION DISPLAY CONNECT THROUGH EXTENDED BRIDGE

and invented by:

Sameh W. Asaad and Kevin W. Warren

If a CONTINUATION APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____

Which is a:

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 16 pages and including the following:
 - a. ☒ Descriptive Title of the Invention
 - b. ☐ Cross References to Related Applications (if applicable)
 - c. ☐ Statement Regarding Federally-sponsored Research/Development (if applicable)
 - d. ☐ Reference to Microfiche Appendix (if applicable)
 - e. ☒ Background of the Invention
 - f. ☒ Brief Summary of the Invention
 - g. ☒ Brief Description of the Drawings (if drawings filed)
 - h. ☒ Detailed Description
 - i. ☒ Claim(s) as Classified Below
 - j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
- a. ☐ Formal Number of Sheets _____
- b. ☒ Informal Number of Sheets **3 (Figs. 1-4)**
4. ☒ Oath or Declaration
- a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
- b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
- c. ☒ With Power of Attorney ☐ Without Power of Attorney
- d. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application,
see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied
under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby
incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
- a. ☐ Paper Copy
- b. ☐ Computer Readable Copy *(identical to computer copy)*
- c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☐ Certificate of Mailing
- ☐ First Class ☐ Express Mail *(Specify Label No.):* _____

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

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Docket No.
YOR9-2000-0175

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Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)

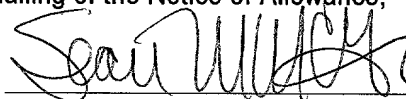
16. ☐ Additional Enclosures (please identify below):

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	21	- 20 =	1	x \$18.00	\$18.00
Indep. Claims	3	- 3 =	0	x \$78.00	\$0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
BASIC FEE					\$690.00
OTHER FEE (specify purpose) Assignment Recordation					\$40.00
TOTAL FILING FEE					\$748.00

- ☒ A check in the amount of \$748.00 to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 50-0481 as described below. A duplicate copy of this sheet is enclosed.
- ☐ Charge the amount of as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).


Signature

Dated: August 7, 2000

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Reg. No.: 34,386

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**APPLICATION
FOR
UNITED STATES
LETTERS PATENT**

APPLICANT: Sameh W. Asaad and Kevin W. Warren

FOR: METHOD AND SYSTEM FOR HIGH
RESOLUTION DISPLAY CONNECT
THROUGH EXTENDED BRIDGE

DOCKET NO.: YOR9-2000-0175

**METHOD AND SYSTEM FOR HIGH RESOLUTION DISPLAY CONNECT THROUGH
EXTENDED BRIDGE**

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application relates to U.S. Patent Application Serial No. __/__, filed on
_____, to Sameh Asaad et al., entitled "METHOD AND SYSTEM FOR
TRANSPORTING SIDEBAND SIGNALS THROUGH PHYSICAL LAYER OF EXTENDED
BRIDGE", having IBM Docket No. YOR9-2000-176US1, and to U.S. Patent Application Serial
No. __/__, filed on _____, to Sameh Asaad et al., entitled
"COMMUNICATIONS SYSTEM INCLUDING SYMMETRIC BUS BRIDGE AND METHOD
USED THEREWITH", having IBM Docket No. YOR9-2000-184US1, and to U.S. Patent
Application Serial No. __/__, filed on _____, to Sameh Asaad et al., entitled
"ALL-IN-ONE MOBILE DOCKING STATION AND SYSTEM USED THEREWITH" having
IBM Docket No. YOR9-2000-0014, and to U.S. Patent Application Serial No. __/__, filed
on _____, to Sameh Asaad, et al., entitled "SYSTEM AND INTELLIGENT DOCK
USING A SYMMETRIC EXTENDED BUS BRIDGE AND METHOD THEREFOR" having
IBM Docket No. YOR9-2000-0015, each of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method and display system for displaying an image with high resolution, and more particularly to a method and display system for displaying an image through an extended Peripheral Component Interconnect (PCI) to PCI bridge.

Description of the Related Art

Figure 1 illustrates a generic architecture for a conventional system 100 including a monitor display 101 connected, via a cable 102, to a personal computer (PC) box 110 including a central processing unit (CPU) and host Peripheral Component Interconnect (PCI) bridge 103 and graphics adaptor 104.

In such systems, there is an increasing trend to replace analog cathode ray tube (CRT) desktop monitors 101 with flat panel display monitors. Various factors contribute to this trend including desktop space saving, power saving, higher resolution and crisper images.

As flat panel display technology pushes towards higher resolutions and actually surpasses the capabilities of current CRT monitors, the question of how to connect the computer to the display becomes an issue.

That is, a problem with the architecture shown in Figure 1 is that the cable 102 from the

graphics adaptor 104 in the PC box 110 to the monitor 101 carries faster information (i.e., pixel by pixel description of the image at 60+ Hz refresh rate) which is too fast for the graphics adaptor 104/monitor 101 to handle efficiently. Thus, the bandwidth requirements increase drastically when increasing the resolution or refresh rate of the monitor 101.

Moreover, for a digitally-driven flat panel monitor, the bandwidth requirement is scaled again by the number of bits per pixel (i.e., color resolution).

Figure 2 summarizes the bandwidth requirements for various common display resolutions, bits per pixel and refresh rates.

From the above, it is clear that connection between the PC and the monitor becomes a bottleneck in the system, especially when digital signals (and thus many more bits/information than analog signals) are sent from the graphics adaptor 104 to the monitor 101. Further, the higher resolution that is provided means that more data which must be displayed.

That is, conventionally, the output of the graphics adaptor has rasterization information (e.g., a matrix of lines and within each of the lines pixel-by-pixel are displayed). As mentioned above, with digital signals becoming more prevalent, more data (e.g., in the form of higher refresh rates, higher pixel counts, a higher number of colors, etc.) will be provided to the graphics adaptor, thereby leading to higher bandwidth requirements and hence the bottleneck. Currently, the monitor is "dumb" and only knows what pixels to place at which point. Thus, the higher resolution displays will cause a severe bottleneck between the graphics adaptor and the monitor.

Additionally, there are electromagnetic induction (EMI) and power dissipation problems.

That is, because this system configuration forces a serial connection, the frequency of transmission is high and this aggravates power and EMI. In addition, the current digital serial display connections are dedicated and "one-way." If there are to be other output devices in the display (speakers, etc.), or input devices (keyboard, mouse, camera, etc.), then other connection mechanisms must be added. These additional connections are not possible with the current dedicated display connections.

Thus, hitherto the present invention, no satisfactory solution has been proposed.

SUMMARY OF THE INVENTION

In view of the foregoing problems, drawbacks, and disadvantages of the conventional systems, it is an object of the present invention to provide a structure and method for using an extended PCI-PCI Bridge (e.g., a PCI-to-PCI or Accelerated Graphic Port (AGP)-to-AGP bridge) for connecting a computer to a display subsystem.

In a first aspect of the present invention, a system and method for displaying information, includes an extended bus bridge, a graphics adaptor coupled to the extended bridge, and a display monitor coupled to the graphics adaptor to display the information, such that the graphics adaptor is localized to the display monitor.

In a second aspect, a display unit includes at least a portion of an extended bus bridge, a graphics adaptor coupled to the at least the portion of the extended bridge, and a display monitor coupled to the graphics adaptor to display the information, such that the graphics adaptor is

localized to the display monitor.

In a third aspect, a method of decreasing a bottleneck in a communications bus, includes providing an extended bus bridge between a graphics adaptor and a central processing unit (CPU), and localizing the graphics adaptor to a display monitor.

5 Generally, the invention provides an extended PCI-PCI (or AGP) Bridge for connecting the computer to the display subsystem.

Moreover, the invention takes the graphics adaptor away from the system PC box and instead places the graphics adaptor with the monitor. Thus, the graphics adaptor is "localized" with the monitor (e.g., placed/positioned with or in the monitor), thereby avoiding the bottleneck caused by the cable having to carry all of the bandwidth of the high resolution image.

Further, in the invention, only information that changes needs to be carried across the cable (e.g., static information which does not change need not be carried continuously across the cable to the graphics adaptor). For example, assuming that a refresh rate of 60 Hz is increased to 80 Hz, then this simply means that more data must be sent since there is no frame buffer or any memory on the monitor side to understand that the refresh rate simply must be increased and the system must increase the rate. However, this operation is not relevant to the graphics adaptor, and thus need not be communicated across the cable to the graphics adaptor. The inventive solution moves the graphics adaptor from the CPU/PC side to the display side, and only information which changes is sent to the graphics adaptor. If the data does not change, then it is not sent to the graphics adaptor, thereby freeing bandwidth. Hence, if a faster refresh is desired, nothing is changed on the cable and thus it is not sent to the graphics adaptor.

Thus, with the unique and unobvious features of the invention, as flat panel display technology pushes towards higher resolutions and surpasses the capabilities of current CRT monitors, the computer can be efficiently and easily connected to the display without any bottleneck being created.

5 That is, even when the bandwidth requirements increase drastically when increasing the resolution or refresh rate of a monitor (e.g., even a digitally-driven flat panel monitor), there is no bottleneck between the connection between the PC and the monitor.

10 Additionally, because the adapter is in the display, the connection between the adapter and the display can be parallel, not serial (e.g., as shown in Figure 3 and described below). This means that the frequency of operation can be reduced and still maintain a high bandwidth. Also, because the high bandwidth connections are local to the display, the EMI can be minimized. Moreover, the EMI characteristics of the cable (e.g., always a large source of radiation) now do not change with frame rate or display type. The characteristics are dependent upon the rate of the bus, which is typically "bursty" but fixed, and thus it is much easier and cheaper to characterize and shield. Because the high bandwidth lines are in the display, their length is made much shorter as well, thereby helping to reduce power. Further, because the connection mechanism is not dedicated to the display and is by its nature "two-way", additional input and output devices can be added to the display by adding additional connection support.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of preferred embodiments of the invention with reference to the drawings, in which:

- 5 Figure 1 illustrates a conventional system 100 having a generic architecture;
- Figure 2 illustrates a cable bandwidth requirement for digital monitor interconnects; and
- Figure 3 illustrates an architecture 300 according to a first preferred embodiment of the present invention; and
- 10 Figure 4 illustrates an architecture 400 according to a second preferred embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

Referring now to the drawings, and more particularly to Figures 3-4, there are shown preferred embodiments of the method and structures according to the present invention.

15 **First Preferred Embodiment**

To attack the above problems of the conventional architectures, the inventive solution extends the PCI bus by using an extended PCI-PCI bridge and colocates the graphics adaptor(s)

with the display itself rather than inside the PC Box 310.

That is, as shown in Figure 3, a system 300 according to the invention includes a PC Box 310 coupled to a display unit 320 via a cable 302. As shown in Figure 3, the invention has moved the graphics adaptor 304 as shown to be a part of the display unit 320 and localized to the monitor 301.

The invention utilizes an extended bus bridge 305. In Figure 3, the bus bridge is shown preferably as a PCI bus bridge 305 having a bus portion 305A on the CPU side and a bus portion 305B on the monitor side. The invention is not limited to the PCI bus bridge and indeed other bus bridges may be employed. For example, as discussed in further detail below, in the second embodiment of the invention, an Accelerated Graphics Port (AGP) bus bridge (e.g., having a bandwidth of 256-512 MBytes/Sec.) may be provided. Additionally, a network bus bridge could be used.

In Figure 3, B0 is the primary side interface of the chip, and it interfaces to the primary PCI bus (bus 0) as a regular PCI-PCI bridge. All PCI traffic addressed to B0 is serialized across a high-speed serial link using, for example, a Gigabit Ethernet as its physical layer.

On the remote side of the serial cable (e.g., up to 30 meters away), interface B1 converts the serial stream back to PCI traffic and relays it to the graphics card (e.g., graphics adaptor 304) now connected to the secondary PCI (bus 1) as shown.

With this embodiment, many advantages accrue to the invention. For example, graphics data on the cable is at the PCI command level, which is at a much lower bandwidth (e.g., maximum of 132 MBytes/sec for a 32bit/33MHz PCI system) than the raster data level.

Further, the required cable bandwidth is constant at the PCI rate irrespective of display resolution, number of bits per pixel or refresh rate. This allows the scaling to high resolution displays with the same architecture.

Further, with the above-mentioned advantage, electromagnetic induction (EMI) issues on the cable are resolved.

Additionally, from a systems perspective, the extended bridge of the invention is transparent. The PC sees a regular PCI-PCI bridge which it is designed to handle. No changes are needed in the graphics adaptor design, system basic input/output system (BIOS), operating system (OS) software, device driver software, or application program.

It is noted that a number of digital interconnects for flat panel displays are in use today, such as PanelLink and digital video interface (DVI). However, none of these digital interconnects employs a system repartitioning as described above, and therefore it is difficult for these schemes to scale up with higher resolution panels.

Further, it is noted that there is no limitation on the type of PC box being used since bus portion B0 is preferably implemented as a modular, add-in card which can be "plugged-in" (e.g., inserted) to the PC similarly to inserting a graphics card.

Second Preferred Embodiment

As mentioned above, the invention is not limited to the PCI bus bridge and indeed other bus bridges may be employed.

For example, as shown in Figure 4, in the second embodiment of the invention, an

Accelerated Graphics Port (AGP) bus bridge may be provided instead of the PCI bus bridge.

Instead of B0 in Figure 3, in Figure 4 a first portion of the AGP bus bridge can be provided on the PC side. Similarly, a second portion of the AGP bus bridge can be provided on the display unit side.

5 Thus, with the unique and unobvious aspects of the present invention, the invention provides an extended PCI-PCI Bridge or an extended AGP bridge for connecting the computer to the display subsystem.

Moreover, the invention takes the graphics adaptor away from the system PC box and instead places the graphics adaptor with the monitor. Thus, the graphics adaptor is localized with the monitor, thereby avoiding the bottleneck caused by the cable having to carry all of the bandwidth of the high resolution image. In the invention, only information that changes need be carried across the cable (e.g., static information which does not change need not be carried continuously across the cable to the graphics adaptor).

Further, as flat panel display technology pushes towards higher resolutions and surpasses the capabilities of current CRT monitors, the computer can be efficiently and easily connected to the display without any bottleneck being created. That is, even when the bandwidth requirements increase drastically when increasing the resolution or refresh rate of a monitor (e.g., even a digitally-driven flat panel monitor), there is no bottleneck between the connection between the PC and the monitor.

20 While the invention has been described in terms of several preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the

spirit and scope of the appended claims.

For example, the present invention is not limited to the PCI or AGP buses. That is, the inventive approach does not require any software changes (e.g., no changes are needed to the PC BIOS, the operating system, the application software systems, etc.). Thus, system components
5 operate as if each is a local element.

However, notwithstanding the above, the invention can be advantageously used by a network as a network display. In a network application, along with the invention, a scheme for translating the traffic which originally went to the network and redirecting the traffic to the network (e.g., Ethernet or other network) card, etc. would be provided such that the graphics information is transported on top of a network and on the back-end another piece of software, hardware, etc. would be employed to reproduce graphics out of network information.

CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A system for displaying information, comprising:

an extended bus bridge;
a graphics adaptor coupled to said extended bus bridge; and
a monitor coupled to said graphics adaptor to display the information, such that said graphics adaptor is localized to said monitor.

2. The system according to claim 1, wherein said extended bus bridge includes first and second portions, a first portion being coupled to said graphics adaptor.

3. The system according to claim 2, further comprising a central processing unit (CPU) coupled to said second portion of said extended bus bridge.

4. The system according to claim 3, further comprising a link for coupling together said first and second portions of said extended bus bridge.

5. The system according to claim 4, wherein said link comprises a serial link.

6. The system according to claim 4, wherein said link comprises at least one of a cable, a radio frequency (RF) link, and an infrared (IR) link.

7. The system according to claim 1, wherein said extended bus bridge comprises a peripheral component interconnect (PCI) bus bridge.

8. The system according to claim 1, wherein said extended bus bridge comprises an Accelerated Graphics Port (AGP) bus bridge.

9. A display unit, comprising:

at least a portion of an extended bus bridge;

a graphics adaptor coupled to said at least portion of the extended bus bridge; and

a monitor coupled to said graphics adaptor to display the information, such that said graphics adaptor is localized to said monitor.

10. The display unit according to claim 9, wherein said at least a portion of said extended bus bridge comprises one side of said extended bus bridge embedded in said adaptor.

11. The display unit according to claim 9, wherein said extended bus bridge includes first and second portions, a first portion being coupled to said graphics adaptor.

12. The display unit according to claim 9, wherein said extended bus bridge comprises a peripheral component interconnect (PCI) bus bridge.

13. The system according to claim 9, wherein said extended bus bridge comprises an Accelerated Graphics Port (AGP) bus bridge.

5 14. A method of decreasing a bottleneck in a communications bus, comprising:
coupling a graphics adaptor, a central processing unit (CPU) and a display monitor over
said communications bus;
providing an extended bus bridge between said graphics adaptor and said central
processing unit (CPU); and
10 localizing said graphics adaptor to said display monitor.

15. The method according to claim 14, wherein said extended bus bridge includes first and second portions, a first portion being coupled to said graphics adaptor.

16. The method according to claim 15, wherein said central processing unit (CPU) coupled to said second portion of said extended bus bridge.

15 17. The method according to claim 16, further comprising coupling together said first and second portions of said extended bus bridge via a link.

18. The method according to claim 17, wherein said link comprises a serial link.

19. The method according to claim 17, wherein said link comprises at least one of a cable, a radio frequency (RF) link, and an infrared (IR) link.

20. The method according to claim 14, wherein said extended bus bridge comprises a peripheral component interconnect (PCI) bus bridge.

21. The method according to claim 14, wherein said extended bus bridge comprises an Accelerated Graphics Port (AGP) bus bridge.

METHOD AND SYSTEM FOR HIGH RESOLUTION DISPLAY CONNECT THROUGH EXTENDED BRIDGE

ABSTRACT OF THE DISCLOSURE

5 A method of (and system for) of displaying information, includes an extended bus bridge,
a graphics adaptor coupled to the extended bridge, and a monitor coupled to the graphics adaptor
to display the information, such that the graphics adaptor is localized to the monitor.

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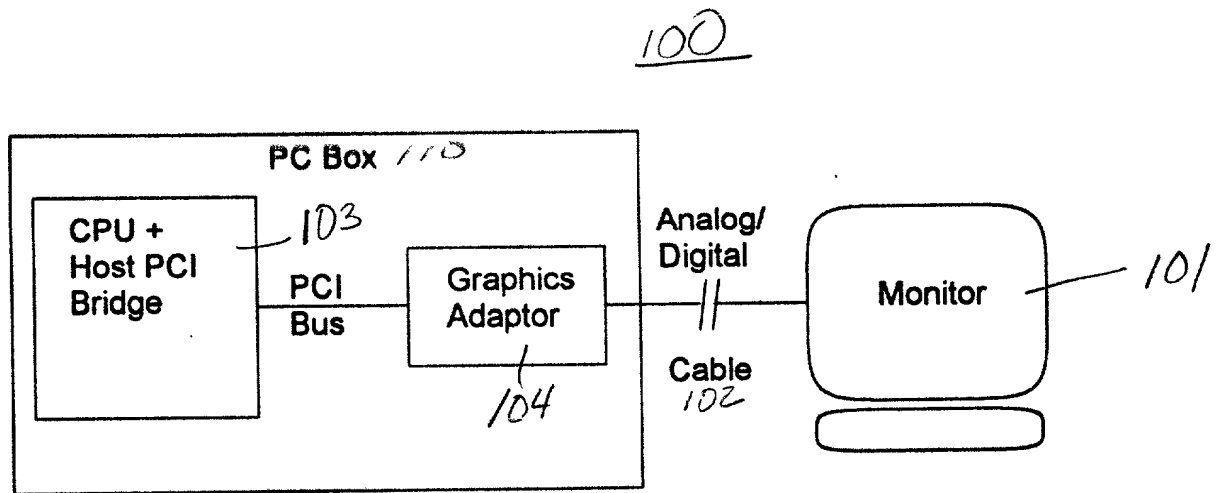


Fig. 1

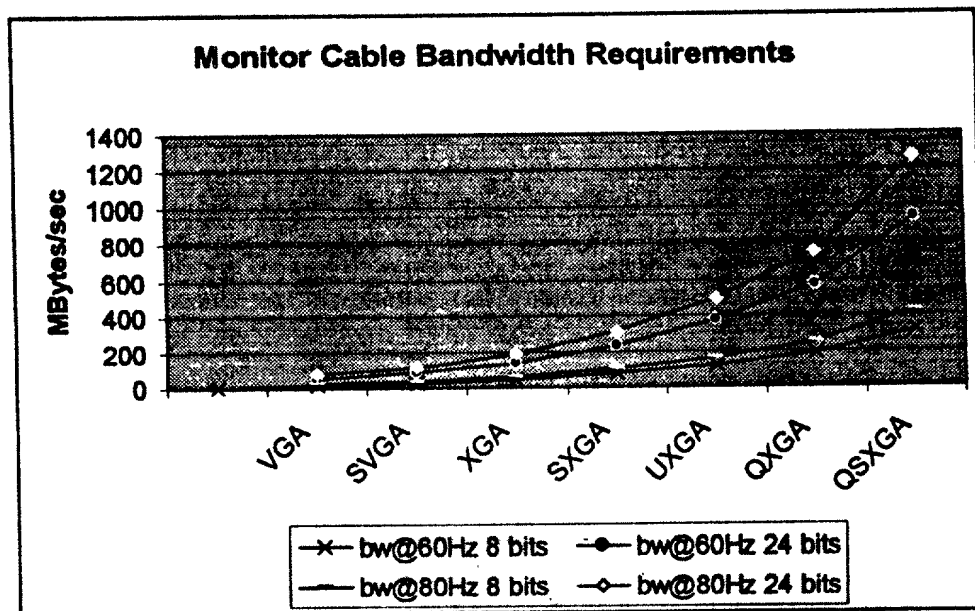


Fig. 2

Figure 1 consists of 12 histograms arranged in a single row. Each histogram represents the frequency distribution of the number of non-zero elements in the vector x for a specific value of n . The x-axis for all histograms is 'Number of non-zero elements in x ' with major ticks at 0, 60, and 120. The y-axis is 'Frequency' with major ticks at 0, 5, and 10. The histograms are labeled with n values: 10, 20, 30, 40, 50, 60, 70, 80, 90, 100, 110, and 120. For $n=10$, the distribution is centered around 60. As n increases, the distribution shifts to the right, indicating a higher number of non-zero elements, and the peak frequency decreases.



Fig. 3

400

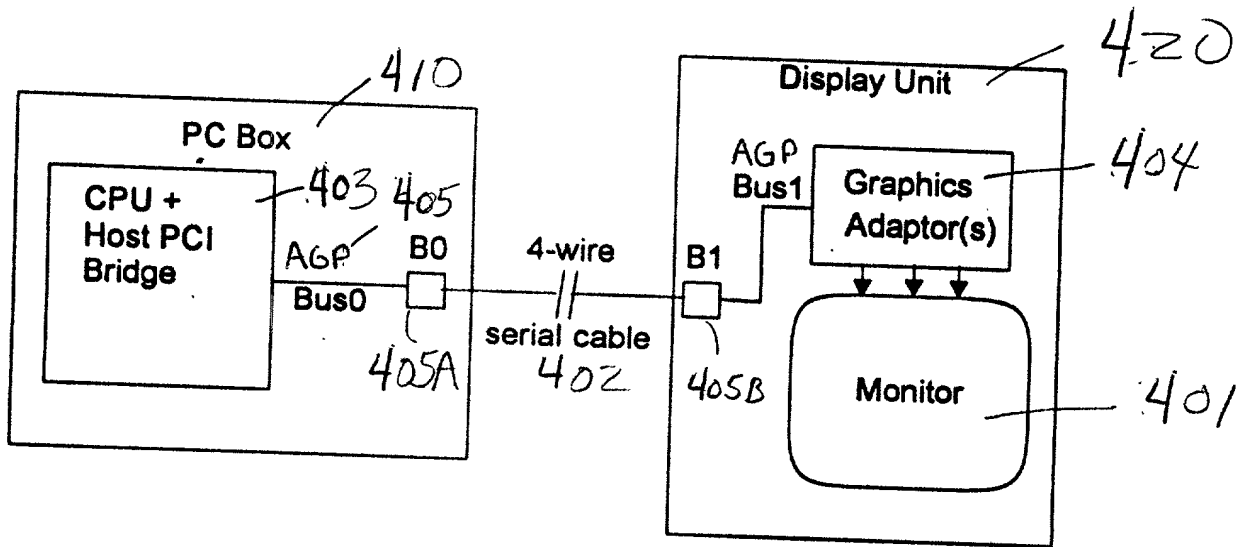


Fig. 4

As a below named inventor, I hereby declare that:

the specification of which:
(check one)

☒ is attached hereto.

☐ was filed on _____, as Application Serial No. _____ and was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

Number	Country	Day/Month/Year	Priority Claimed
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I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Applications:

Serial No.	Filing Date	Status
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: We hereby appoint Manny Schechter, Registration No. 31,722, Christopher A. Hughes, Registration No. 26,914, Edward A. Pennington, Registration No. 32,588, John E. Hoel, Registration No. 26,279, Joseph C. Redmond, Jr., Registration No. 18,753, Douglas W. Cameron, Registration No. 31,596, Wayne L. Ellenbogen, Registration No. 43,602, Louis P. Herzberg, Registration No. 41,500, Stephen C. Kaufman, Registration No. 29,551, Daniel P. Morris, Registration No. 32,053, Louis J. Percello, Registration No. 33,206, David M. Shofi, Registration No. 39,835, Paul J. Otterstedt, Registration No. 37,411, Robert M. Trepp, Registration No. 25,933, and Lauren Bruzzone, Registration No. 35,082 to prosecute this application and transact all business in the United States Patent and Trademark Office connected therewith.

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(2) Inventor: Kevin W. Warren

Signature:  Date: 7/31/2000

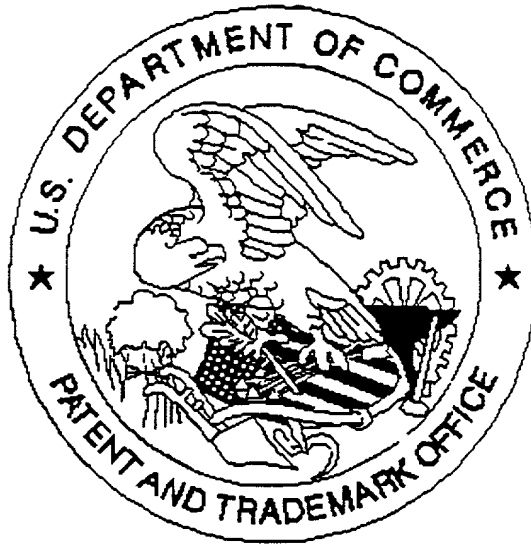
Residence: 8 Rega Road, Fishkill, NY 12524

Citizenship: United States of America

Post Office Address: Same as Residence

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Application deficiencies were found during scanning:

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